What Is Claimed Is:

1. A method for a serial transmission of data between a processor module and at least one peripheral element, comprising:

transmitting a timing signal via two timing lines between the processor module and the at least one peripheral element;

transmitting a data signal via two data lines between the processor module and the at least one peripheral element; and

transmitting a selection signal via the two data lines.

2. The method of claim 1, wherein:

the data signal is transmitted on a first data line; and

an inverted data signal is transmitted on a second data line.

3. The method of claim 2, wherein:

the timing signal is transmitted on a first timing line; and

an inverted timing signal is transmitted on a second timing line.

4. The method of claim 1, wherein a symmetry of transmission of the data signal is violated for transmitting the selection signal.

5. The method of claim 4, further comprising:

synchronizing the at least one peripheral element by using a symmetry violation between two transmitted data words.

6. The method of claim 4, wherein:

at least one specified bit is transmitted between two defined symmetry violations; and

the at least one specified bit is used to address the at least one peripheral element.

7. The method of claim 6, wherein an address space for addressing the at least one peripheral element is predefined by varying a time interval between the two defined symmetry violations.

8. A device for a processor module for serial transmission of data between the processor module and at least one peripheral element, comprising:

a first arrangement for transmitting a timing signal via two timing lines between the processor module and the at least one peripheral element;

a second arrangement for transmitting a data signal via two data lines between the processor module and the at least one peripheral element; and

a third arrangement for transmitting a selection signal via the two data lines.

9. The device of claim 8, wherein the data signal is transmitted on a first data line, and an inverted data signal is transmitted on a second data line.

10. The device of claim 8, wherein the device is a serial-peripheral-interface-bus interface.

11. A processor module, comprising:

a device for a serial transmission of data between the processor module and at least one peripheral element;

wherein the device transmits a timing signal via two timing lines between the processor module and the at least one peripheral element;

wherein the device transmits a data signal via two data lines between the processor module and the at least one peripheral element; and

wherein the device transmits a selection signal via the two data lines.

12. The processor module of claim 11, wherein the data signal is transmitted on a first data line, and an inverted data signal is transmitted on a second data line.

13. The method of claim 1, wherein the processor module is a control unit of a motor vehicle.

14. The device of claim 8, wherein the processor module is a control unit of a motor vehicle.

15. The processor module of claim 11, wherein the processor module is a control unit of a motor vehicle.